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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental Office Action Summary	Application No. 10/718,008	Applicant(s) DONG ET AL.	
	Examiner Thanh Y. Tran	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 11, 14, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Kunori (U.S. 2003/0100153).

As to claim 1, Kunori discloses in figures 1-3 a method comprising:

(a) defining a first oxidation stop layer (top portion of "silicon nitride film" 3) above a first conductively-doped semiconductor layer (1);

(b) providing a first intrinsic silicon layer (30) (paragraph [0064]) on the first oxidation stop layer (top portion of "silicon nitride film" 3);

(c) oxidizing at least a sublayer portion of the first intrinsic silicon layer (30) so as to thereby create a corresponding and thermally-grown, first intrinsic silicon oxide sublayer (4) over the first semiconductor layer (1) (see paragraphs [0064]-[0065] & [0070]); and

(d) disposing a second conductively-doped semiconductor layer (6) above the first intrinsic silicon oxide sublayer (4) so that the first intrinsic silicon oxide sublayer (4) provides isolation between the first and second conductively-doped semiconductor layers (1, 6).

As to claim 11, Kunori discloses in figures 1-3 a method, comprising the step of: continuing said oxidizing of the first intrinsic silicon layer (30) yet further so as to consume

silicon atoms within the first oxidation stop layer (top portion of 3) and so as to thereby produce additional silicon oxide from the consumed silicon atoms.

As to claim 14, Kunori discloses in figures 1-3 a method, comprising the steps of: providing a silicon nitride layer (bottom portion of 3) between the first and second conductively-doped semiconductor layers (1, 6) so that the combination of the silicon nitride layer (bottom portion of 3) and the first intrinsic silicon oxide sublayer (4) provide isolation between the first and second conductively-doped semiconductor layers (1, 6).

As to claim 22, Kunori discloses in figures 1-3 a method comprising:

(a) defining a first oxidation stop layer (top portion of "silicon nitride film" 3) above a first conductively-doped semiconductor layer (1);

(b) providing an essentially undoped semiconductor layer (30) on the first oxidation stop layer (top portion of "silicon nitride film" 3) (see paragraph [0064]);

(c) oxidizing at least a sublayer portion of the essentially undoped semiconductor layer (30) so as to thereby create a corresponding, essentially undoped and thermally-grown, first oxide sublayer (4) over the first conductively-doped semiconductor layer (1); and

(d) disposing a second conductively-doped semiconductor layer (6) above the first oxide sublayer (4) so that the first oxide sublayer (4) provides electrical isolation between the first and second semiconductor layers (1, 6).

3. Claims 2-4, 10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunori (U.S. 2003/0100153) in view of Lee et al. (US 2005/0074982).

As to claim 2, Kunori does not disclose the thermally-grown, first intrinsic silicon oxide sublayer includes stoichiometric silicon dioxide (SiO.sub.2).

Lee et al discloses the intrinsic silicon oxide ("thermal oxide layer") includes SiO_2 (see paragraph [0006]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Kunori by having an intrinsic silicon oxide which includes SiO_2 as taught by Lee for providing a stable silicon dioxide thermal layer with the underlying silicon substrate, and a fabrication process which is relatively simple (see paragraph [0006] in Lee).

As to claim 3, Kunori does not disclose a providing step of the first intrinsic silicon layer includes using atomic layer deposition (ALD) to define a thickness of the first intrinsic silicon layer. Lee et al. disclose a providing step of the first intrinsic silicon layer includes using atomic layer deposition (ALD) to define a thickness of the first intrinsic silicon layer (see paragraph 46). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Kunori by using atomic layer deposition (ALD) for defining a thickness of the layer as taught by Lee et al for the purpose of controlling the thickness of the layer (see paragraph [0046] in Lee).

As to claim 4, Kunori does not disclose the thickness of the first intrinsic silicon layer is in a range of about 15 Angstroms to about 50 Angstroms. Lee et al. disclose said thickness of the first intrinsic silicon layer is in a range of about 15 Angstroms to about 50 Angstroms (wherein the controlled thickness are in the range of approximately 2-60 angstroms (see col. 5, claim 6). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Kunori by providing a thickness range of about 15 Angstroms to about 50 Angstroms as taught by Lee for providing a controlled thickness for a desirable layer (see claim 6 in Lee).

As to claims 10 and 12, Kunori discloses in figures 1-3 a method, comprising the steps of: continuing said oxidizing of the first intrinsic silicon layer (30) at least until a corresponding first oxidation front crosses into the first oxidation stop layer (top portion of 3); providing silicon nitride layer (bottom portion of "silicon nitride film" 3) between the first and second conductively-doped semiconductor layers (1, 6) so that the combination of the silicon nitride layer (bottom portion of 3) and the perfected silicon oxide in the thermally-oxidized, first intrinsic silicon layer (30) provide isolation between the first and second conductively-doped semiconductor layers (1,6).

Kunori does not disclose the formation of silicon dioxide in the thermally-oxidized, first intrinsic silicon layer.

Lee et al discloses a formation of silicon dioxide ("silicon dioxide thermal oxide layer") in the thermally-oxidized, first intrinsic silicon layer ("silicon substrate") (see paragraph [0006]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Kunori by having a formation of silicon dioxide in the thermally-oxidized, first intrinsic silicon layer as taught by Lee et al for providing a stable silicon dioxide thermal layer with the underlying silicon substrate, and a fabrication process which is relatively simple (see paragraph [0006] in Lee).

As to claim 13, Kunori discloses in figures 1-3 a method, comprising the steps of: providing a second silicon oxide layer (2), the silicon nitride layer (bottom portion of "silicon nitride film" 3) and the second conductively-doped semiconductor layer (6) so that the combination of the second silicon oxide layer (2), the silicon nitride layer (bottom portion of

"silicon nitride film" 3) and the perfected silicon oxide (4) in the thermally-oxidized, first intrinsic silicon layer (30) provide isolation between the first and second conductively-doped semiconductor layers (1, 6).

Kunori does not disclose silicon dioxide in the thermally-oxidized intrinsic silicon layer.

Lee et al discloses silicon dioxide ("silicon dioxide thermal oxide layer") in the thermally-oxidized intrinsic silicon layer ("silicon substrate") (see paragraph [0006]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Kunori by having a silicon dioxide in the thermally-oxidized intrinsic silicon layer as taught by Lee et al for providing a stable silicon dioxide thermal layer with the underlying silicon substrate, and a fabrication process which is relatively simple (see paragraph [0006] in Lee).

Kunori in view of Lee et al does not disclose the step of: providing a second silicon oxide layer *between* the silicon nitride layer and the second conductively-doped semiconductor layer. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Kunori in view of Lee et al by rearranging the second silicon oxide layer which is positioned between the silicon nitride layer and the second conductively-doped semiconductor layer for providing the isolation between the conductively-doped semiconductor layers, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

4. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunori (U.S. 2003/0100153) in view of Lee et al. (US 2005/0074982) as applied to claims 1, and 3-4 above, and further in view of Yamazaki et al (US 2005/0040401).

As to claims 5 and 6, Kunori in view of Lee et al. (US 2005/0074982) does not disclose said defining of the first oxidation stop layer includes creating a first silicon nitride composition having a nitrogen concentration of at least about 5% or 10% atomic.

Yamazaki et al. disclose said defining of the first oxidation stop layer includes creating a first silicon nitride composition ("silicon nitride oxide film 602a"; figures 6A-8C; paragraph [0125]) having a nitrogen concentration of at least about 5% or 10% atomic (adjusted to at least 25 atomic % to less than 50 atomic %; paragraph [0125]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Kunori in view of Lee by providing a percentage range of at least about 5% or 10% atomic of nitrogen concentration in silicon nitride composition as taught by Yamazaki for the purpose of obtaining an optimized operation during a heat-treatment of the semiconductor device.

5. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunori (U.S. 2003/0100153) in view of Lee et al (US 2005/0074982) and Yamazaki et al (US 2005/0040401) as applied to claims 1, and 3-5 above, and further in view of Yu et al. (US 6566205).

As to claims 7 and 8, Kunori in view of Lee et al and Yamazaki et al does not disclose the step of: creating of the first silicon nitride composition includes using Decoupled Plasma

Nitridation (DPN) or Remote Plasma Nitridation (DPN) to introduce nitrogen into the first conductively-doped semiconductor layer.

Yu et al. discloses the step of: creating of the first silicon nitride composition includes using Decoupled Plasma Nitridation (DPN) or Remote Plasma Nitridation (DPN) to introduce nitrogen into the first conductively-doped semiconductor layer (see column 2, lines 13-16; column 3, lines 28-35). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Kunori in view of Lee et al and Yamazaki et al by using Decoupled Plasma Nitridation (DPN) or Remote Plasma Nitridation (DPN) to introduce nitrogen into the conductively-doped semiconductor layer as taught by Yu et al for the purpose of obtaining a FET gate capable of operating at low voltages and having a minimum of trapped charge in a dielectric portion (see column 2, lines 13-16; column 3, lines 28-35).

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kunori (U.S. 2003/0100153) in view of Lee et al. (US 2005/0074982) and Yamazaki et al. (US 2005/0040401) as applied to claims 1, and 3-5 above, and further in view of Noguchi et al (U.S. 2004/0094793).

As to claim 9, Kunori in view of Lee et al and Yamazaki et al does not disclose the step of: creating of the first silicon nitride composition includes using ion implant to introduce nitrogen into the first conductively-doped semiconductor layer.

Noguchi et al discloses the step: creating of the first silicon nitride ("silicon nitride film") composition includes using ion implant to introduce nitrogen into the conductively-doped semiconductor layer (see paragraph [0155]). Therefore, it would have been obvious to a person

having ordinary skill in the art at the time the invention was made to modify the method of Kunori in view of Lee et al and Yamazaki et al by using ion implant for creating a silicon nitride as taught by Noguchi et al for performing the isolation film (see paragraph [0155] in Noguchi et al).

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kunori (U.S. 2003/0100153).

As to claim 15, Kunori discloses in figures 1-3 a method, comprising the steps of: providing a second silicon oxide layer (2), the silicon nitride layer (bottom portion of "silicon nitride film" 3), and the second conductively-doped semiconductor layer (6) so that the combination of the second silicon oxide layer (2), the silicon nitride layer (bottom portion of "silicon nitride film" 3) and the first intrinsic silicon oxide sublayer (4) provide isolation between the first and second conductively-doped semiconductor layers (1, 6).

Kunori does not disclose the step of: providing a second silicon oxide layer *between* the silicon nitride layer and the second conductively-doped semiconductor layer. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Kunori in view of Lee et al by rearranging the second silicon oxide layer which is positioned between the silicon nitride layer and the second conductively-doped semiconductor layer for providing the isolation between the conductively-doped semiconductor layers, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Miura et al (U.S. 6,649,542) discloses multi-level type nonvolatile semiconductor memory device.

Kunikiyo (U.S. 6,661,065) discloses semiconductor device and SOI substrate.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zandra V. Smith
Supervisory Patent Examiner
31 March 2006

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